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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/973,795	10/11/2001	Kazuya Ono	A319-1	7244

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EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/973,795	ONO, KAZUYA	
	Examiner	Art Unit	
	Michael C Maskulinski	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/24/04; 11/7/03;*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS: 7/23/04; 10/11/01*.

Non-Final Office Action

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2, 6, 7, 10, 11, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Kageyama et al., U.S. Patent 4,110,558.

Referring to claims 1 and 10:

a. In column 9, lines 45-51, Kageyama et al. disclose that after a 512-bit test data block is fed to the modulator, three check bits stored in the shift register are fed to the modulator (a check bit producer which applies an error correcting code to parallel data transmitted through said parallel bus).

b. In column 9, lines 21-56, Kageyama et al. disclose a parallel-in serial-out shift register for the 512 data bits and the 3 check bits (a parallel-serial converter which converts said parallel data output from said check bit producer, into serial data).

Referring to claim 2:

a. In column 9, lines 21-56, Kageyama et al. teach a parallel bus interface circuit which multiplexes said parallel data transmitted through said parallel bus, in predetermined bits, and outputs the thus multiplexed parallel data to said check bit producer. Further, in column 9, lines 21-56, Kageyama et al. disclose a

parallel-in serial-out shift register for the 512 data bits and the 3 check bits (said parallel-serial converter converts said parallel data into serial data every said predetermined bits).

b. In column 9, lines 45-51, Kageyama et al. disclose that after a 512-bit test data block is fed to the modulator, three check bits stored in the shift register are fed to the modulator (said check bit producer applies said error correcting code to every said predetermined bits of said parallel data).

Referring to claims 6 and 15:

a. In column 9, lines 45-51, Kageyama et al. disclose that after a 512-bit test data block is fed to the modulator, three check bits stored in the shift register are fed to the modulator (a check bit producer which applies an error correcting code to parallel data transmitted through said parallel bus).

b. In column 9, lines 21-56, Kageyama et al. disclose a parallel-in serial-out shift register for the 512 data bits and the 3 check bits (a parallel-serial converter which converts said parallel data output from said check bit producer, into serial data).

c. In column 10, lines 7-9, Kageyama et al. disclose that a backward signal from the receiving side is entered into a serial-in parallel-out shift register (a serial-parallel converter which converts serial data transmitted through said serial bus, into parallel data).

d. In column 11, lines 12-49, Kageyama et al. disclose that the last three bits of a count value counted by the counter are applied to a comparator. Thus

comparison is made in the comparator between a number of "1" bits included in each test data block and the check bits (an error detector which checks an error-correcting code applied to said serial data, and detects an error in said error correcting code).

Referring to claim 7:

a. In column 9, lines 21-56, Kageyama et al. teach a parallel bus interface circuit which multiplexes said parallel data transmitted through said parallel bus, in predetermined bits, and outputs the thus multiplexed parallel data to said check bit producer and receives parallel data from said error detector, and outputs the received parallel data to said parallel bus. Further, in column 9, lines 21-56, Kageyama et al. disclose a parallel-in serial-out shift register for the 512 data bits and the 3 check bits (said parallel-serial converter converts said parallel data into serial data every said predetermined bits).

b. In column 9, lines 45-51, Kageyama et al. disclose that after a 512-bit test data block is fed to the modulator, three check bits stored in the shift register are fed to the modulator (said check bit producer applies said error correcting code to every said predetermined bits of said parallel data).

Referring to claims 11 and 16:

a. In column 9, lines 21-56, Kageyama et al. teach multiplexing said parallel data transmitted through said parallel bus, in predetermined bits. Further, in column 9, lines 21-56, Kageyama et al. disclose a parallel-in serial-out shift

register for the 512 data bits and the 3 check bits (said parallel-serial converter converts said parallel data into serial data every said predetermined bits).

b. In column 9, lines 45-51, Kageyama et al. disclose that after a 512-bit test data block is fed to the modulator, three check bits stored in the shift register are fed to the modulator (said check bit producer applies said error correcting code to every said predetermined bits of said parallel data).

3. Claims 3-5, 12-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Götze et al., U.S. Patent 4,450,561.

Referring to claims 3 and 12:

a. In Figures 1 and 2, Götze et al. teach a serial communication device bridging between a parallel bus and a serial bus.

b. In column 4, lines 29-32, Götze et al. disclose that serially arriving data bits are read into a shift register for serial-parallel conversion. Data arriving in parallel are read into the ECC (a serial-parallel converter which converts serial data transmitted through said serial bus, into parallel data).

c. In column 2, lines 61-68 continued in column 3, lines 1-4, Götze et al. disclose that upon the read-out, check bits for the read-out data are generated and these check bits are compared with the stored check bits. The comparison of two corresponding check bits results in the so-called syndrome bit. If all syndrome bits are 0 it can be assumed that the read-out data are identical with the previously read-in data, i.e. that the data have not been adversely affected. If one or several syndrome bits are not 0, this indicates a single error or a double

error depending on the encoding rule selected for generating the check bits (an error detector which checks an error correcting code applied to said serial data, and detects an error in said error correcting code).

Referring to claims 4 and 13, in column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector has a function of correcting said error when said error is detected by said error detector).

Referring to claims 5 and 14, in column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector corrects said error when said error is a 1-bit error). Further, in column 6, lines 39-42, Götze et al. disclose that a double error can be detected but not corrected (said error detector abandons an access when said error is a 2-bit error).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 6, 8-10, 15, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Götze et al., U.S. Patent 4,450,561, and further in view of Carlton et al., U.S. Patent 4,218,742.

Referring to claims 1 and 10:

a. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence (applying an error correcting code to parallel data transmitted through said parallel bus).

b. In Figure 4, Götze et al. disclose outputting the check bits in parallel, however, Götze et al. don't explicitly disclose a parallel-serial converter which converts said parallel data output from said check bit producer, into serial data. In column 1, lines 12-18, Carlton et al. disclose that various arrangements are known in the art fro transferring data which is received at a disk file controller in parallel by bit form to a disk file in serial by bit form to be written on one of the tracks. It would have been obvious to one of ordinary skill at the time of the invention to include the parallel-serial conversion of Carlton et al. into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to include ECC bits when writing and reading data to insure data integrity. Therefore, ECC bits of Götze et al. would be needed in the system of Carlton et al. Further, the system of Carlton et al. provides a means of changing the parallel ECC bits into a serial stream that can be used by most disk drives.

Referring to claims 6 and 15:

a. In column 1, lines 49-52, Götze et al. disclose that each of the check bits of an ECC codeword is generated in parallel in a byte serial sequence (a check bit producer which applies an error correcting code to parallel data transmitted through said parallel bus).

b. In Figure 4, Götze et al. disclose outputting the check bits in parallel, however, Götze et al. don't explicitly disclose a parallel-serial converter which converts said parallel data output from said check bit producer, into serial data. In column 1, lines 12-18, Carlton et al. disclose that various arrangements are known in the art fro transferring data which is received at a disk file controller in parallel by bit form to a disk file in serial by bit form to be written on one of the tracks. It would have been obvious to one of ordinary skill at the time of the invention to include the parallel-serial conversion of Carlton et al. into the system of Götze et al. A person of ordinary skill in the art would have been motivated to make the modification because it is important to include ECC bits when writing and reading data to insure data integrity. Therefore, ECC bits of Götze et al. would be needed in the system of Carlton et al. Further, the system of Carlton et al. provides a means of changing the parallel ECC bits into a serial stream that can be used by most disk drives.

c. In column 1, lines 15-18, Carlton et al. disclose the reverse process of transferring the serial by bit data stream generated by reading the stored data from the file controller in parallel by bit form (a serial-parallel converter which converts serial data transmitted through said serial bus, into parallel data).

d. In column 2, lines 61-64, Götze et al. disclose that upon the read-out, the check-bits fro the read-out data are generated and these check bits are compared with the stored check bits (an error detector which checks an error

correcting code applied to said serial data, and detects an error in said error correcting code).

Referring to claims 8 and 17, in column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector has a function of correcting said error when said error is detected by said error detector).

Referring to claims 9 and 18, in column 3, lines 4-6, Götze et al. disclose that most ECC devices are structured in such a manner that single errors can be corrected (said error detector corrects said error when said error is a 1-bit error). Further, in column 6, lines 39-42, Götze et al. disclose that a double error can be detected but not corrected (said error detector abandons an access when said error is a 2-bit error).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent 4,171,765	Lemone
U.S. Patent 4,622,670	Martin
U.S. Patent 5,077,656	Waldron et al.
U.S. Patent 5,357,531	Tanaka
U.S. Patent 5,946,327	Murphy

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael C Maskulinski whose telephone number is (571) 272-3649. The examiner can normally be reached on Monday-Friday 9:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MM

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